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SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Toshiyuki Motooka, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan, Yoshiyuki Yoneda, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan, Ryuji Nomoto, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan, Toshimi Kawahara, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan and Junichi Kasai, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan have invented certain new and useful improvements in

SEMICONDUCTOR DEVICE HAVING A BALL GRID
ARRAY AND A FABRICATION PROCESS THEREOF

of which the following is a specification : -

1 TITLE OF THE INVENTION

 SEMICONDUCTOR DEVICE HAVING A BALL GRID
ARRAY AND A FABRICATION PROCESS THEREOF

5 BACKGROUND OF THE INVENTION

 The present invention generally relates to
semiconductor devices having a ball grid array (BGA)
contact structure and more particularly to a so-called
micro-BGA device in which a circuit substrate is
10 provided on a semiconductor chip with a size smaller
than an outer dimension of the semiconductor chip.

 FIG.1 shows a conventional semiconductor
device having a BGA contact structure.

 Referring to FIG.1, the semiconductor device
15 includes a circuit substrate 36 and a semiconductor
chip 32 provided on a top surface of the circuit
substrate 36. Further, electrodes on the
semiconductor chip 32 are electrically interconnected
to corresponding electrodes formed on the top surface
20 of the circuit substrate 36 by way of a bonding wire
34. The electrodes on the top surface of the circuit
substrate 36 are in turn interconnected to respective
corresponding electrodes on a bottom surface of the
circuit substrate 36 via through-holes (not shown)
25 provided in the circuit substrate 36. The circuit
substrate 36 further carries solder bumps 37 on the
bottom surface in correspondence to the electrodes
provided thereon. The semiconductor chip 32 on the
top surface of the circuit substrate 36 is
30 encapsulated by a resin package body 31 together with
the bonding wire 34.

 FIG.2 shows another conventional BGA
semiconductor device disclosed in the United States
Patent 5,148,265.

35 Referring to FIG.2, the BGA semiconductor
device is distinct over the semiconductor device of
FIG.1 in that a circuit substrate 46 corresponding to

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1 the circuit substrate 36 of FIG.1 is now provided on a
top surface of a semiconductor chip 42 corresponding
to the semiconductor chip 32, with a size smaller than
an outer size of the semiconductor chip 42. Such a
5 BGA device that uses a circuit substrate having an
outer size smaller than the outer size of a
semiconductor chip is called a micro-BGA device. In
the micro-BGA device of FIG.2, it should be noted that
the solder bumps (not shown) are provided on
10 electrodes 43 formed on the circuit substrate 46.

11 In the foregoing conventional BGA device of
FIG.1, there arises a problem in that, because of the
lateral size of the circuit substrate exceeding the
size of the semiconductor chip, the overall size of
15 the semiconductor device tends to become excessively
large and a high-density mounting of the device on an
electronic apparatus is difficult.

In the foregoing micro-BGA device of FIG.2,
on the other hand, it is necessary to bond the circuit
20 substrate, of which size is smaller than a size of the
semiconductor chip, on the semiconductor chip, while
handling or alignment of such a small semiconductor
chip or small circuit substrate is difficult and
increases the number of fabrication steps as well as
25 the cost of the semiconductor device.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the
present invention to provide a novel and useful
30 semiconductor device and a fabrication process thereof
wherein the foregoing problems are eliminated.

Another and more specific object of the
present invention is to provide a semiconductor device
including a semiconductor chip and a circuit
35 substrate, wherein the semiconductor device has an
outer size substantially identical with an outer size
of the semiconductor chip, and wherein the circuit

1 substrate is attached to the semiconductor chip by a
simple and easy process.

Another object of the present invention is
to provide a method of fabricating a semiconductor
5 device, comprising the steps of:

forming an electronic circuit on a wafer in
a region defined by a scribe line, said wafer carrying
a first electrode thereon;

10 attaching a circuit substrate carrying
thereon a predetermined conductor pattern, on said
wafer, said circuit substrate carrying a second
electrode and a third electrode, said step of
attaching said circuit substrate including a step of
aligning said circuit substrate with respect to said
15 electronic circuit in said wafer;

interconnecting said first electrode on said
wafer and second electrode of said predetermined
conductor pattern by a wire bonding process;

forming a spherical electrode on said third
20 electrode; and

dicing said wafer along said scribe line.

Another object of the present invention is
to provide a semiconductor device, comprising:

25 a semiconductor chip having a top surface,
said semiconductor chip carrying a first electrode;

a circuit substrate attached to a top
surface of said semiconductor chip, said circuit
substrate carrying thereon a predetermined conductor
pattern including a second electrode and a third
30 electrode;

a resin layer intervening between said top
surface of said semiconductor chip and said circuit
substrate;

35 a spherical electrode provided on said
circuit substrate in correspondence to said third
electrode;

a bonding wire electrically interconnecting

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1 said second electrode of said predetermined conductor
pattern on said circuit substrate and said first
electrode on said semiconductor chip; and

5 a resin potting encapsulating said bonding
wire including said first and second electrodes,
said chip and said resin potting being
defined by a common edge surface substantially
perpendicular to a principal surface of said
substrate.

10 Another object of the present invention is
to provide a semiconductor device, comprising:

a semiconductor chip having a top surface,
said semiconductor chip carrying a first electrode;

15 a circuit substrate attached to a top
surface of said semiconductor chip, said circuit
substrate carrying thereon a predetermined conductor
pattern including a second electrode and a third
electrode;

20 a spherical electrode provided on said
circuit substrate in correspondence to said third
electrode;

25 a bonding wire electrically interconnecting
said second electrode of said predetermined conductor
pattern on said circuit substrate and said first
electrode on said semiconductor chip;

a resin potting encapsulating said bonding
wire including said first and second electrodes;

a resin side wall cover covering a side wall
of said circuit substrate;

30 said chip having a side wall substantially
flush to an outer surface of said resin side wall
cover, said side wall of said chip being substantially
perpendicular to a principal surface of said chip.

35 According to the present invention, the
semiconductor wafer, in which a number of
semiconductor chips are formed as an integral
monolithic body, is diced after the circuit substrate

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1 is attached thereto. Thereby, the adjustment for a
proper positioning between the chip and the circuit
substrate is achieved easily for each chip by merely
conducting a positioning adjustment between the
5 semiconductor wafer as a whole and a master circuit
substrate that includes the circuit substrates with a
large number in a mechanically interconnected state.

Other objects and further features of the
present invention will become apparent from the
10 following detailed description when read in
conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE INVENTION

FIG.1 is a diagram showing the construction
15 of a conventional semiconductor device;

FIG.2 is a diagram showing the construction
of another conventional semiconductor device;

FIG.3 is a diagram showing the construction
of a semiconductor device according to a first
20 embodiment of the present invention;

FIG.4 is a diagram showing the construction
of the semiconductor of FIG.3 in an oblique view with
a part thereof removed;

FIGS.5A - 5F are diagrams showing a
25 fabrication process of the semiconductor device of the
first embodiment;

FIGS.6A and 6B are diagrams showing a
modified fabrication process of the semiconductor
device of the first embodiment;

FIG.7 is a diagram showing a fabrication
30 process of a semiconductor device according to a
second embodiment of the present invention;

FIG.8 is a diagram showing the semiconductor
device of the second embodiment in a cross-sectional
35 view;

FIG.9 is a diagram showing the semiconductor
of the second embodiment in an oblique view;

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1 FIG.10 is a diagram showing the construction
of a semiconductor device according to a third
embodiment of the present invention; and
 FIGS.11A - 11F are diagrams showing the
5 fabrication process of the semiconductor device of the
third embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT
[FIRST EMBODIMENT]

10 FIG.3 shows a semiconductor device 5
according to a first embodiment of the present
invention in a cross-sectional view, while FIG.4 shows
the same semiconductor device 5 formed on a
semiconductor wafer 2A such as a Si wafer in an
15 oblique view for a state before the semiconductor
wafer 2A is diced into individual semiconductor chips
2 along a scribe line 2B.

 Referring to FIG.3, the semiconductor device
5 is constructed on the semiconductor chip 2 and
20 includes a circuit substrate 6 that is provided on the
semiconductor chip 2, with an intervening adhesive
layer 3a that causes the circuit substrate 6 to adhere
to the semiconductor chip 2 firmly. The chip 2
carries thereon an electrode pad 8a that is connected
25 electrically to a corresponding electrode pad 8b on
the circuit substrate 6 by way of a bonding wire 4.
Further, the bonding wire 4 is embedded in a resin
potting 1.

 In the construction of the semiconductor
30 device 5 of the present embodiment, the electrical
signal appearing on the electrode pad 8a of the chip 2
is forwarded to the electrode pad 8b on the circuit
substrate 6 by way of a bonding wire 4 and further to
an electrode pad 8c on the circuit substrate 6 by way
35 of a conductor pattern 9 provided on the circuit
substrate 6. The electrode pad 8c carries thereon a
spherical or semi-spherical solder bump 7 or a

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1 suitable spherical electrode. It should be noted that
the conductor pattern 9 on the circuit substrate 6 is
covered by a solder resist layer 3b, and the solder
bump 7 projects outwardly from the solder resist layer
5 3b that covers the surface of the circuit substrate 6.
It should be noted that the layer 3b is not
illustrated in FIG.3.

It should be noted that the semiconductor
chip 2 is fabricated according to a standard
10 fabrication process of an integrated circuit and
supplies the output electrical signal to the electrode
pad 8a provided thereon.

On the other hand, the adhesive layer 3a is
formed of an adhesive material constituted by a
15 principal resin component and a solvent that dissolves
a flexibilizer. For example, a reactive thermoplastic
resin that contains a carboxyl group or a denatured
maleic acid anhydride may be used for the principal
resin, while a reactive silicone such as a silicone
20 having an epoxy group may be used for the
flexibilizer.

More specifically, a bisphenol A-type epoxy
resin may be used for a binder resin of the adhesive
layer 3a in combination with a suitable amount of
25 phenol novolak resin, which is used as a curing agent.
The binder and the curing agent are then diluted by
butylcellosolve acetate and mixed by a rolling
process. Further, sieved Al particles having an
average diameter in the range of 3 - 30 μm are added
30 further to the mixture thus obtained, with a
proportion such that the adhesive layer contains, in a
completely cured state thereof, the Al particles with
a proportion of about 30 vol%. The target adhesive is
then obtained by adding triphenylphosphine further to
35 the mixture as a cure accelerator, shortly before the
end of the roll mixing process, with a proportion of
about 2 wt% with respect to the 100 wt% of the epoxy

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1 resin.

2.3 The bonding wire 4, on the other hand, may
be formed of a wire of gold or aluminum having a
diameter of 25 - 30 μ m and is bonded to the electrode
5 8a or 8b by using an ordinary wire bonding apparatus.
In the present invention, a first bonding process is
conducted to the electrode 8a on the chip, followed by
a second bonding process that is conducted to the
electrode 8b, for reducing the overall height of the
10 semiconductor device 5.

The circuit substrate 6 is formed of a glass
epoxy or polyimide and is bonded to the semiconductor
chip 2 by way of the adhesive layer 3a as indicated in
FIG.3. It should be noted that the circuit substrate
15 6 carries thereon the conductor pattern 9, such that
the conductor pattern 9, which may be formed of Cu,
extends from the electrode 8b to the electrode 8c on
which the solder bump 7 is formed. The conductor
pattern 9 can be formed in any desired shape by
20 conducting an etching process.

The solder bump 7 is typically formed of an
alloy containing 60 wt% of Sn and 40 wt% of Pb,
wherein the composition of the solder bump 7 may be
adjusted appropriately depending upon the necessary or
25 desired characteristics of the solder bump. Thus, the
solder bump 7 may contain other elements than Sn or
Pb. Further, the solder bump 7 may be formed by
plating a solder alloy around a spherical or semi-
spherical core of Cu or a resin.

30 FIGS.5A - 5F show the fabrication process of
the BGA device 5 of FIG.3.

Referring to FIG.5A, the adhesive layer 3a
is provided on a top surface of a semiconductor wafer
10, wherein the semiconductor wafer 10 includes a
35 number of electronic devices in respective regions
each defined by a scribe line 51 and corresponding to
a chip, as a monolithic integral body. The adhesive

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1 layer 3a is formed by a suitable process such as a
screen printing process that uses a metal mask or a
screen mask. Alternatively, the adhesive layer 3a may
be formed by a potting process.

5 Next, in the step of FIG.5B, a master
circuit substrate 6A is mounted on the adhesive layer
3a, wherein the master circuit substrate 6A includes a
number of the circuit substrates 6 in a mechanically
interconnected state by a bridging part 6B. The
10 master circuit substrate 6A is thereby adjusted with
respect to the electronic devices formed on the wafer
10 such that each of the circuit substrates 6 included
in the master circuit substrate 6A achieves a proper
alignment to the corresponding electronic device on
15 the wafer 10. Thereafter, the adhesive layer 3a is
cured and the master circuit substrate 6A is firmly
attached to the wafer 10 via the adhesive layer 3a.
In the construction of FIG.5B, it should be noted that
there is formed a groove in correspondence to the
20 scribe line 51 such that the top surface of the wafer
10 is exposed at the groove 51.

Of course, it is possible to form the master
circuit substrate 6A first and attach the
semiconductor wafer 10 to the circuit substrate 6A by
25 interposing the adhesive layer 3a therebetween.

Next, in the step of FIG.5C, the electrode
pads (not shown) on the wafer 10 exposed by the groove
51 are interconnected to corresponding electrode pads
on the master circuit substrate 6A by respective
30 bonding wires 4, by conducting a wire bonding process
in each of the regions of the wafer 10 and in each of
the circuit substrates 6 included in the master
circuit substrate 6A. Preferably, the wire bonding
process of FIG.5C is conducted first by bonding an end
35 of the bonding wire 4 to an electrode pad on the wafer
10, followed by bonding an opposite end of the bonding
wire 4 to an electrode pad on the master circuit

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1 substrate 6A. By doing so, it becomes possible to
reduce the loop height of the bonding wire 4.

Next, in the step of FIG.5D, the bonding
wire 4 is embedded into the resin potting 1, which is
5 provided along the scribe line 51 as indicated in
FIG.5D, and the solder bumps 7 are formed on the top
surface of the master circuit substrate 6A as
indicated in FIG.5E. The solder bump 7 is formed
easily by causing a reflowing of a solder ball which
10 is placed on the electrode pad 8c shown in the oblique
view of FIG.4. By covering the solder ball by a flux
layer and transferring the flux layer to the electrode
pad 8c, the formation of the semi-spherical solder
bump 7 is achieved successfully upon reflowing of the
15 solder ball.

The structure thus obtained is then diced in
the step of FIG.5F by applying a dicing saw 50 along
the dicing line 51, and the semiconductor device 5 of
FIG.3 is obtained. As a result of the foregoing
20 dicing process, the semiconductor wafer 10 is divided
into individual semiconductor chips 2. Similarly, the
master circuit substrate 6A is divided into individual
circuit substrates 6.

The semiconductor device 5 thus formed has a
25 characteristic feature that the side wall of the
semiconductor chip 2 forms a flush surface with a side
wall of the resin potting 1 and that the side wall of
the semiconductor chip 2 is substantially
perpendicular to the principal surface of the
30 semiconductor chip 2. Further, the foregoing
fabrication process, particularly the dicing process
of FIG.5F is advantageous for avoiding the problem of
chipping of the semiconductor chip, by protecting the
semiconductor wafer by the resin potting 1 along the
35 scribe line 51.

FIG.6A shows a preferable modification of
the wire bonding process of FIG.5C conducted by a

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1 bonding tool 52, in which the master circuit substrate
6A includes a depressed region adjacent to the scribe
line 51, and it can be seen that an electrode pad 8b
is formed on such a depressed region. As indicated in
5 FIG.6A, the electrode pad 8b is connected to a
corresponding electrode 8a on the wafer 10 by the
bonding wire 4. The construction of FIG.6A is
advantageous for reducing the loop height of the
bonding wire 4.

10 FIG.6B shows a part of the semiconductor
device that is formed from the half-product of FIG.6A.

Referring to FIG.6B, it can be seen that the
semiconductor device has an advantageous feature in
that the bonding wire 4, and hence the resin potting 1
15 holding the bonding wire 4 therein, is substantially
accommodated in the depression formed at the edge of
the circuit substrate 6A facing the scribe line 51.
Thus, the risk that the solder bumps 7 on the top
surface of the circuit substrate 6A failing to make a
20 contact with an external electronic device due to the
projection of the resin potting 1 is positively
eliminated. Associated therewith, it should be noted
that the size or diameter of the solder bumps 7 can be
reduced without causing a problem of failure of
25 contact with the external electronic device.

As already noted, the present invention as
set forth above with reference to the first embodiment
successfully eliminates the complex and time-consuming
alignment process for achieving a proper alignment
30 between a semiconductor chip and a corresponding
minute circuit substrate, and the efficiency of
production of the BGA semiconductor device is improved
substantially.

35 [SECOND EMBODIMENT]

FIG.7 shows a fabrication process of a BGA
semiconductor device 15 according to a second

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1 embodiment of the present invention.

Referring to FIG.7, the semiconductor wafer 10 carries an adhesive layer 13a corresponding to the adhesive layer 3a, and a master circuit substrate 16A is provided on the adhesive layer 13a in correspondence to the master circuit substrate 6A of FIG.5F. Further, spherical or semi-spherical solder bumps 17 are provided on the top surface of the master circuit substrate 16A in correspondence to the solder bumps 17.

In the present embodiment, the groove 51 formed in the master circuit substrate 16A and exposing the top surface of the wafer 10 is not used for the scribe line, and the electrode pads on the exposed top surface of the wafer 10 along the groove 51 are connected electrically to corresponding electrode pads on the master circuit substrate 16A by way of respective bonding wires 14. The bonding wires 14 are further embedded into a resin potting 11.

In the present embodiment, a groove 61 is formed at a location bisecting the region of the master circuit substrate 16A located between a first groove 51 and an adjacent groove 51, and the dicing is conducted along the groove 61 by applying a dicing saw to the groove 61 in a state that the groove 61 is filled by a resin potting similar to the resin potting 1.

FIG.8 and 9 show the BGA semiconductor device 15 of the present embodiment in detail respectively in a cross sectional view and in an oblique view for a state after the dicing process is conducted.

Referring to FIGS.8 and 9, it should be noted that electrode pads 18a corresponding to the electrode pads 8a are provided on the exposed top surface of the chip 12, wherein the chip 12 is formed as a result of dicing of the wafer 10 along the scribe

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1 lines 61 of FIG.7.

2 The electrode pads 18a are formed in the
3 groove in a criss-cross pattern, and each electrode
4 pad 18a is connected to a corresponding electrode pad
5 18b provided on the top surface of the circuit
6 substrate 16, which is obtained as a result of the
7 dicing of the master circuit substrate 16A, by a
8 bonding wire 14. The circuit substrate 16 further
9 carries a number of conductor patterns 19 each
10 extending between an electrode pad 18a and an
11 electrode pad 18c, wherein the electrode pad 18c is
12 provided on the top surface of the master circuit
13 substrate 16A and hence on the top surface of the
14 circuit substrate 16 in correspondence to the
15 electrode pad 8c of FIG.4. Further, the top surface
16 of the circuit substrate 16 is protected by a solder
17 resist 13b except for the part where the solder bumps
18 17 are formed.

19 In the BGA device of the present embodiment,
20 the bonding wires 14 are used to connect the
21 corresponding electrode pads 18a and the electrode
22 pads 18b at a central part of the chip 12, as
23 indicated in FIG.8. Further, the BGA semiconductor
24 device of the present invention is laterally
25 surrounded by the resin potting 1.

26 The fabrication process of the BGA device of
27 the present invention is substantially identical with
28 that of the BGA device of the first embodiment, except
29 that there is a difference in the shape of the circuit
30 substrate 16 or in the location of the groove in which
31 the wire bonding is made.

32 The present embodiment is advantageous in
33 the point that it enables a saving of the area that is
34 used for achieving the wire bonding process.

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[THIRD EMBODIMENT]

FIG.10 shows the construction of a BGA

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1 semiconductor device 25 fabricated according to a
third embodiment of the present invention.

Referring to FIG.10, the semiconductor
device 25 includes a circuit substrate 26
5 corresponding to the circuit substrate 6, wherein the
circuit substrate 26 is formed of a polyimide film
carrying thereon a conductor pattern and is mounted on
a semiconductor chip 22 corresponding to the
semiconductor chip 2 without an intervening adhesive
10 layer. The conductor pattern on the polyimide film 26
may be formed by an etching process. On the polyimide
film 26, there are provided a plurality of semi-
spherical solder bumps 27 in correspondence to the
solder bumps 7 on the circuit substrate 6. The
15 foregoing conductor pattern on the polyimide film 26
is connected to the electrode pads on the
semiconductor chip 22 by way of bonding wires 24.
Further, the bonding wires 24 are embedded in a resin
potting 21, wherein it should be noted that the resin
20 potting 21 further supports the polyimide film 26 on
the top surface of the semiconductor chip 22.

Hereinafter, the fabrication process of the
BGA device 25 of the present invention will be
described with reference to FIGS.11A - 11F.

25 Referring to FIG.11A, the polyimide film 26,
which carries thereon the conductor pattern, is
aligned with respect to the Si wafer 10. In FIG.11A,
it should be noted that the polyimide film 26 forms a
continuous film as indicated by a broken line. On the
30 other hand, the polyimide film 26 includes a cutout in
correspondence to the broken line, and the top surface
of the Si wafer 10 is exposed at the foregoing cutout.
It should be noted that the polyimide film 26 is
disposed on the wafer 10 such that the cutout is
35 aligned with the scribe line 51 defined in the wafer
10.

The polyimide film 26 thus aligned is then

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1 fixed temporarily on the wafer 10 by a jig such as a
clip as indicated in FIG.11B, and a wire bonding
process is conducted in the step of FIG.11C by using
the bonding wire 24. Thereby, the length of the
5 bonding wire 24 is set to be slightly larger than the
length needed in the wire bonding process conducted in
the state of FIG.11C.

Next, an injection of the resin 21 is
conducted in the step of FIG.11D along a periphery of
10 the wafer 10, and the polyimide film 26 is lifted in
the upward direction from the wafer 10 as indicated in
FIG.11D as a result of such an injection of the resin
21. Thereby, the length of the bonding wire 24 is
chosen such that the polyimide film 26 can be lifted
15 freely in the upward direction with a predetermined
distance. Such an injection of the resin 21 is easily
implemented by using an apparatus that is used
conventionally in the mounting process of a flip-chip
package device or a BGA package device for introducing
20 an under-fill resin between the mounting substrate and
the chip or a BGA package.

After the step of FIG.11D, the solder bumps
27 are formed on the corresponding electrode pads of
provided on the polyimide film 26 as indicated in
25 FIG.11E, and the structure of FIG.11E is diced in the
step of FIG.11F along the scribe lines by applying a
dicing saw 50. As a result of the dicing step of
FIG.11F, the BGA device 25 of FIG.10 is obtained in
which it should be noted that the chip 22 and the
30 resin body 21 have a common, flush side wall
perpendicular to the principal surface of the chip 22.

In the dicing step of FIG.11F, it should be
noted that the dicing of the semiconductor wafer 10 is
conducted in the state that the wafer 10 is protected
35 by the resin 21. Thus, the problem of chipping of the
diced semiconductor chip 22 is effectively avoided.

In the present embodiment, too, it should be

1 noted that the proper alignment between the individual
chip 22 and the polyimide circuit substrate 26 is
achieved easily, by conducting such an alignment
process before the semiconductor wafer 10 is divided
5 into individual semiconductor chips 22. Further, the
present embodiment can eliminate the process of
applying an adhesive film on the wafer 10.

Further, the present invention is by no
means limited to the embodiments described heretofore,
10 but various variations and modifications may be made
without departing from the scope of the invention as
set forth in claims.

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